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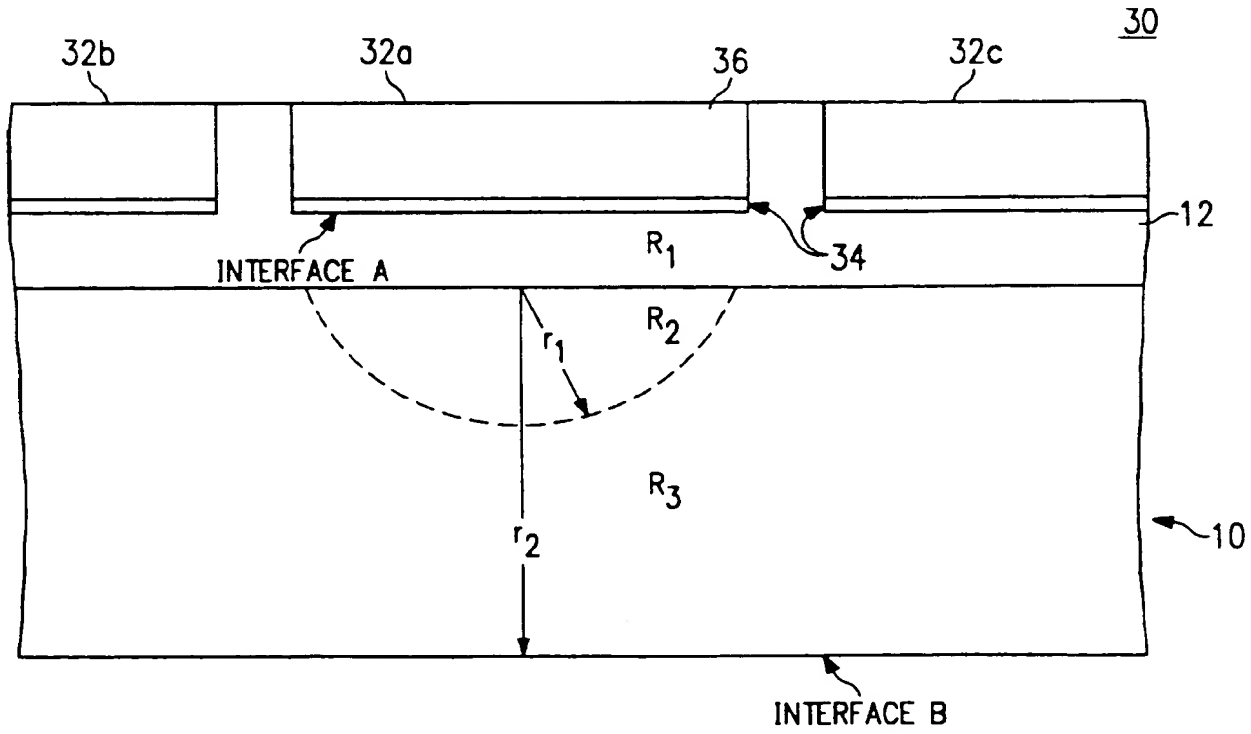

(57) **Abstract**

An integrated circuit structure containing dielectrically isolated islands having heat dissipation paths of enhanced thermal conductivity. A semiconductor structure comprises a first layer of crystalline material with a layer comprising polycrystalline diamond formed over the first layer. A layer of polycrystalline silicon is formed over the diamond containing layer and a layer of monocrystalline material is formed over the polycrystalline silicon.

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SILICON ON DIAMOND CIRCUIT STRUCTURE AND METHOD OF MAKING SAME

FIELD OF THE INVENTION

This invention relates to integrated circuitry of the type formed with electrically isolated devices and, more particularly, to a dielectrically isolated structure providing improved circuit capabilities.

BACKGROUND OF THE INVENTION

A variety of techniques have been employed to achieve device isolation in integrated circuitry. These include junction isolation, formation of channel stops with dopant implants and the inclusion of dielectric material, e.g., by local oxidation of silicon. For the silicon planar process the class of dielectric isolation commonly referred to as *silicon on insulator* (SOI), is used to form individual devices on discrete islands or mesas. Advantages of SOI technology include improved power handling capability, avoidance of latch-up problems associated with junction isolation, and improvements in transistor operating frequency, the latter resulting from lower output capacitance attributable to the dielectric isolation. Generally SOI structures exhibit greater tolerance and immunity to the effects of ionizing radiation and, therefore, are the structure of choice for rad hard environments.

In the past, such dielectrically isolated islands have been formed by thermally growing an oxide layer on a silicon wafer surface and then depositing a relatively thick layer of polycrystalline silicon (polysilicon) over the oxide. The

polysilicon layer, sometimes referred to as the handle, is relied upon to provide structural integrity to the overall wafer during subsequent processing. The silicon wafer material is frequently thinned to a thickness of less than 1 mil and polished to provide a starting material for epitaxial silicon growth. This technique is characterized by relatively high temperature processing, consequent high levels of mechanical stress, lattice damage and various nonuniformities across the wafer. See, however, U.S. Patent No. 4,554,059, assigned to the assignee of the present invention, which teaches an electrochemical technique for improving the wafer yield of integrated circuits formed with dielectrically isolated islands.

Several other SOI techniques are of current interest. These include Separation by IMplantation of OXygen (SIMOX), Zone Melt Recrystallization (ZMR), Full Isolation by the Porous Oxidation of Silicon (FIPOS), Silicon on Sapphire (SOS) and bonded wafers. At this time, SOS and bonded wafer technology have advanced sufficiently to realize commercial feasibility.

A feature common to all of the aforementioned SOI technologies is the relatively low thermal conductivity characteristic of the insulator material. Thus, design considerations based on upper limits for steady state operating temperatures of active devices frequently require inclusion of a cooling zone, i.e., additional heat dissipation volume, within each device island. In addition to having a significant

impact on the achievable level of device integration, the added volume of semiconductor material can increase parasitic capacitance thereby degrading overall circuit performance. By way of example, consider that the area size of a bipolar transistor island permits a predetermined level of power dissipation beyond which the operating temperature becomes undesirably high relative to ambient conditions. For one known geometry with island dimensions of 51 microns by 43 microns, a temperature rise on the order of 1° C will occur with 1.5 mW of steady state power dissipation. In order to increase the power dissipation to 3.75 mW, while still limiting the temperature to 1° C above ambient, it becomes necessary to increase the island dimensions to 81 microns by 73 microns. That is, approximately 2.5 times the surface area is required in order to dissipate the additional heat. In circuits employing high speed transistors, the required cooling zone can impart other undesirable effects such as parasitic collector-substrate capacitance. Such capacitance such can reduce the circuit frequency response by 20%.

From the above it is apparent that competing demands for increased power handling capability and higher levels of device integration require application specific tradeoffs. This is particularly problematic in view of the current trends to develop standard cell libraries and device arrays each suitable for a wide variety of applications.

SUMMARY OF THE INVENTION

There is now provided an integrated circuit structure containing dielectrically isolated islands having heat dissipation paths of enhanced thermal conductivity. Generally, the integrated circuit structure comprises a first layer of crystalline material and a layer of polycrystalline diamond formed thereover. Polycrystalline silicon is formed over the diamond layer and a layer of monocrystalline semiconductor material is formed over the polycrystalline silicon. In the preferred embodiments, the first layer of crystalline material is a single crystal semiconductor material such as silicon or a compound semiconductor; and the layer of monocrystalline material formed over the polycrystalline silicon is, preferably, a single crystal wafer bonded to the polysilicon.

A method for forming an integrated circuit structure having heat dissipation paths of enhanced thermal conductivity includes forming a layer of polycrystalline diamond over a first surface of a layer of substrate material. A polycrystalline silicon layer is formed over the polycrystalline diamond and a layer of monocrystalline semiconductor material is formed over the polycrystalline silicon.

The interest in employing diamond material as a passive component in an integrated circuit structure is, of course, not new. Growth of single crystal diamond films has not been demonstrated. Moreover, significant lattice mismatch has

precluded epitaxial growth of silicon films over monocrystalline diamond.

Efforts to use polycrystalline films in order to realize the electrical and thermal benefits of diamond have previously had significant drawbacks that made high volume commercialization difficult. For example, subsequent to deposition of the diamond film on a silicon wafer, a relatively thick, e.g., 20 mil, polysilicon layer is normally deposited to form a structural backing. Such a backing, or wafer handle, is needed to sustain the integrity of the relatively thin epitaxial silicon layer after thinning or removal of substrate silicon. High temperature processing of the thick polycrystalline handle layer is believed to contribute to wafer warpage.

DESCRIPTION OF THE FIGURES

For a more complete understanding of the invention, reference is made to the following description in conjunction with the accompanying drawings wherein:

Figures 1 through 3 illustrate various stages during formation of a semiconductor structure according to the invention.

Figure 4 illustrates a preferred embodiment of the invention.

Figure 5 is a partial view of an integrated circuit structure according to the invention; and

Figure 6 is a schematic illustration of a circuit formed with the structure of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

An exemplary process sequence is illustrated in Figures 1-3. Fabrication begins with preparation of a wafer substrate for receiving polycrystalline diamond over a surface thereof. Figure 1 illustrates a monocrystalline silicon wafer 10 having a thin polycrystalline layer 12 formed over a wafer surface 14. For example, a diamond film ranging from 1 to 5 microns in thickness can be deposited by DC, RF or Microwave Plasma Enhanced Chemical Vapor Deposition (CVD) at a deposition pressure ranging from 5 to 100 TORR and at a temperature in the range of 600 C to 1000 C. For a more detailed discussion on techniques for forming diamond films on non-diamond substrates, see Zhu, et al. "Growth and Characterization of Diamond Films on Nondiamond Substrates for Electronic Applications" Proceedings of the IEEE, Vol. 79, No. 5, May 1991.

With reference to Figure 2, a thin polycrystalline silicon layer 16, e.g., 1 to 2 microns thick, is next formed over the diamond layer 12. Most preferably, the polysilicon material is formed with a low pressure, chemical vapor deposition technique at a relatively low temperature, e.g., in the range of 600 C. Alternately, the deposition can be had by Plasma Enhanced CVD. Thickness of the polysilicon film 16 could be significantly less than 1 micron, and, for example, on the order of 0.1 micron, depending on the smoothness of the underlying diamond

surface. Generally, sufficient polycrystalline silicon is formed over the diamond surface to assure satisfactory bonding of the overall structure with a second wafer. It is desirable to minimize stress effects between the polycrystalline silicon film 16 and underlying material and thereby minimize warpage. The film 16 should therefore be of minimum thickness. Of course, by minimizing surface roughness of the diamond layer 12, one can further reduce the thickness of the polysilicon film 16. Choice of a low deposition temperature when forming the film 16 also reduces residual stress.

Next, the polysilicon film is polished to provide a smooth bonding surface for receiving a second wafer. This can be effected with well known techniques such as with a chemical/mechanical polish employing colloidal silica to provide a planar mirror finish.

A crystalline silicon wafer 18, having a smooth polished surface 20 with planarity comparable to that of the film 16, is then bonded to the polysilicon film 16. See Figure 3. Techniques for bonding a monocrystalline surface with a polycrystalline silicon surface are known. See Jones, et. al., Abstract No. 478, J. Electrom. Soc., Vol. 138, No. 8, August 1991. Bonding should be preceded by a pre-bond surface treatment consisting of, for example, an $H_2SO_4\backslash H_2O_2$ cleaning followed by a second cleaning with NH_4OH and a spin rinse/dry. Enhanced bonding between the polysilicon layer 16 and the wafer surface 20 may be had by formation of oxide at the interface.

For example, inclusion of a liquid oxidant, such as water, in a high temperature anneal, e.g., above 900 C, in a neutral ambient environment for several hours results in an oxygen bond between lattice silicon and polycrystalline silicon. For further details see U.S. Patent No. 4,962,062 issued October 09, 1990 and incorporated herein by reference. See, also, U.S. Patent Application Serial No. 07/834,439, continuation of Serial No. 476,322, filed 2/7/90, assigned to the assignee of the present invention and incorporated herein by reference, disclosing a preferred liquid oxidant for enhancing bonded wafer yield.

If it is desirable to direct bond the polysilicon layer 16 to the wafer 18 without retaining a residual intervening oxide layer, then such bonding may be accomplished by growing the wafer 18 by the float-zone (FZ) method and allowing only native oxide on the surface of the polysilicon film 16 and the wafer surface 20. The surfaces are placed in contact with one another and the structure is annealed at a high temperature. The native oxide will dissolve into the FZ wafer during the anneal because FZ silicon has an extremely low oxygen content. This method of bonding may be desirable when devices are to be fabricated on the side of the bonded structure containing the polysilicon layer 16.

Devices and circuits may be formed on the bonded wafer structure 22 of Figure 3 with standard processes. Subject to choice of materials, devices may be formed on either or both

the substrate 10 and the wafer 18 of the resulting structure for integrated circuit formation. For example, the wafer layer 18 can be ground back and polished to a thickness on the order of 1 micron for subsequent formation of a heavily doped layer underlying subsequent epitaxial growth. Device formation on the side of the bonded wafer having the polysilicon material between the layer 18 and the diamond layer 12 can enhance circuit performance. That is, the polysilicon will getter metallic impurities and crystalline defects. Moreover, low minority carrier lifetime, a characteristic of the polysilicon region, can minimize photocurrent generation in a transient ionizing radiation environment.

The silicon on diamond structure 22 provides several features advantageous to the planar process. The diamond film is an excellent insulator exhibiting a dielectric constant of 5.5 and an electrical resistivity on the order of 10^{16} ohm cm. On the other hand, the diamond film exhibits a thermal conductivity on the order of 20 W/cm K. As indicated in the table below, this provides a substantial improvement over the thermal properties characteristic of other materials used in semiconductor circuits.

Semiconductor or Insulator Material Type	Thermal Conductivity W/(cm K)
Si	1.4
SiO_2	0.014
Si_3N_4 (silicon nitride)	0.185
Al_2O_3 (sapphire)	0.3
diamond	20.

ADVANTAGES AND MODIFICATIONS

Figure 4 illustrates (not to scale) a SOI structure 30 according to the invention, comprising a plurality of rectangular device islands 32 formed over a layer 12 of diamond insulator. Each device island 32 comprises a lower portion 34 corresponding to the polycrystalline silicon layer 16 and an upper portion 36 corresponding to the bonded wafer layer 18 and epitaxial material formed thereon. The device islands 32 may be considered circular in order to simply illustrate advantages of the invention. Other geometries are more common.

The thermal resistance $R_{AB} = R_1 + R_2 + R_3$, corresponds to a thermal conduction path extending from the interface A, between device island 32a and the diamond layer 12, to an interface B at the lower surface of the crystalline silicon handle substrate 10. Assuming that the interface A is circular, R_1 corresponds to the portion of the path extending from the interface A through the diamond layer 12; and R_2 corresponds to

a hemispherical portion of the path extending into the substrate 10 from the interface between the substrate and the diamond layer 12. In a first order linear approximation, the hemispherical portion is assumed to have a radius r_1 equivalent to the radius of a circular interface A with the overlying device island 32a. R_3 corresponds to the thermal resistance associated with the remaining thermal conduction path through the substrate 10 to the interface B. The thermal resistances could be approximated as follows:

$$R_1 = \frac{d}{\sigma_1(\pi r_1^2)}$$

$$R_2 = \frac{r_1}{\sigma_{si}(\pi r_1^2)} = \frac{1}{\sigma_{si}\pi r_1} \quad \text{(linear approximation)}$$

$$R_3 = \frac{1}{2\pi\sigma_{si}} \left(\frac{1}{r_1} - \frac{1}{r_2} \right)$$

wherein: d = insulator thickness in cm

σ_1 = insulator thermal conductivity (W/cm K)

r_1 = radius of circular interface A

r_2 = substrate thickness

σ_{si} = silicon thermal conductivity

By way of example, there may be an insulator thickness, d, of 2 x 10^{-4} cm, an INTERFACE A radius r_1 of 30 x 10^{-4} cm and a substrate thickness, r_2, of 254 x 10^{-4} cm. If the dielectric material of the structure 30 was silicon dioxide instead of the diamond layer 12, the resulting thermal resistance R_{AB} would be 614 K/W. However, with the diamond film 12 the thermal

resistance of the structure 30 between INTERFACE A and INTERFACE B is only 109 K/W.

For a power dissipation of 3.75 mW, the resulting temperature rise with respect to ambient is on the order of 0.4 C. In contrast, the same power dissipation in a structure formed with silicon dioxide dielectric instead of the diamond layer 12 would exhibit a temperature rise of approximately 2.3 C above ambient.

From the above example, it is apparent that the SOI structure 30 will allow for substantial increases in power dissipation without requiring dedication of additional semiconductor area for thermal dissipation.

Figure 5 illustrates in partial cross-sectional view integrated circuitry on the structure 30. Devices formed on the islands 32 may be connected into the NAND gate schematically illustrated in Figure 6. With reference to Figures 4, 5 and 6, NAND gate transistor Q1A is formed on island 32a and NAND gate transistor Q1B is formed on island 32c. Each transistor includes a N^- collector region 38 formed in the monocrystalline upper portion 36 and a buried N^+ region 40 formed in polycrystalline silicon lower portion 34. N+ collector contacts 42 extend from the island surface, through the upper portion 36, and down to the buried layer 40. The base regions 44 and emitter regions 46 are formed over the collector regions 38 by implantation and diffusion. See U.S. Patent Application Serial No. 07/766,201, filed 9/27/91,

incorporated herein by reference. Interconnect 45, such as may be formed with a metal level or polysilicon deposition, connects the base region 44 of Q1A to the base region 44 of transistor Q1B. Lateral isolation is provided between the islands 32 with a combination SiO_2 44 and trench filled polysilicon 46, both extending down to the polydiamond layer 12. Further isolation and passivation are provided with a thermally grown oxide layer 48 and a deposited oxide 50, respectively.

Based on the above description, various modifications and alternate embodiments will be apparent. Accordingly, the invention is only to be limited by the claims which follow:

CLAIMS

I claim:

1. A method for forming an integrated circuit structure having a plurality of transistors formed in electrically isolated regions, comprising the steps of:

providing a first layer of substrate material;

forming a layer of polycrystalline diamond over a first surface of the substrate material;

forming a polycrystalline silicon layer over the polycrystalline diamond layer; and

forming a layer of monocrystalline semiconductor material over the polycrystalline silicon layer.

2. The method of Claim 1 wherein the layer of monocrystalline semiconductor material is a wafer predominantly comprising silicon and the step of forming said layer over the polycrystalline silicon layer is accomplished by bonding the wafer to the polycrystalline silicon layer.

3. The method of Claim 2 wherein the wafer is bonded to the polycrystalline silicon by forming an intervening oxide of silicon.

4. A semiconductor structure comprising:

a first layer of crystalline material having a first surface;

a layer comprising polycrystalline diamond formed over the first surface;

a layer of silicon formed over the diamond layer; and

a layer of monocrystalline semiconductor material formed over the layer of silicon.

5. The structure of Claim 4 wherein the layer of silicon comprises polycrystalline silicon and the layer of monocrystalline semiconductor material includes a first surface bonded to the layer of polycrystalline silicon by intervening oxide bonds.

6. The structure of Claim 4 wherein the layers of silicon and monocrystalline semiconductor material are patterned to form multiple electrically isolated device islands, said structure further including a plurality of transistors each formed on a device island, said transistors connected to provide an integrated circuit.

7. The structure of Claim 4 wherein the transistors are connected to provide a logic function.

8. The structure of Claim 4 wherein the layer of silicon is polycrystalline silicon and the layer of monocrystalline semiconductor material is a crystalline silicon wafer suitable for formation of electronic devices and circuits.

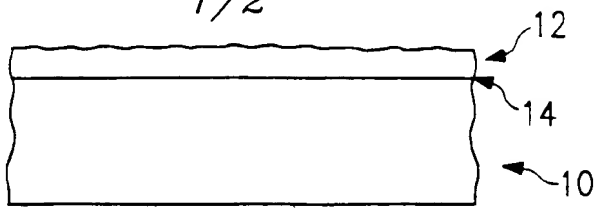

FIG. 1

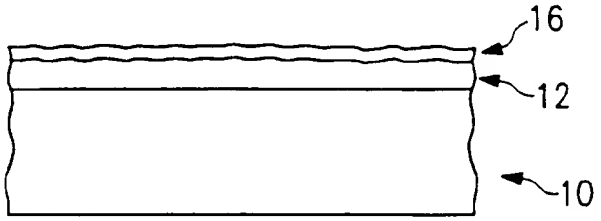

FIG. 2

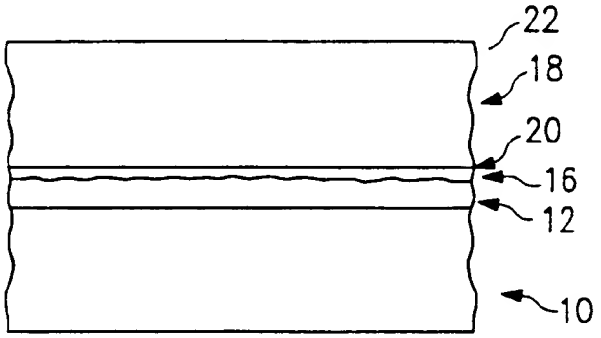

FIG. 3

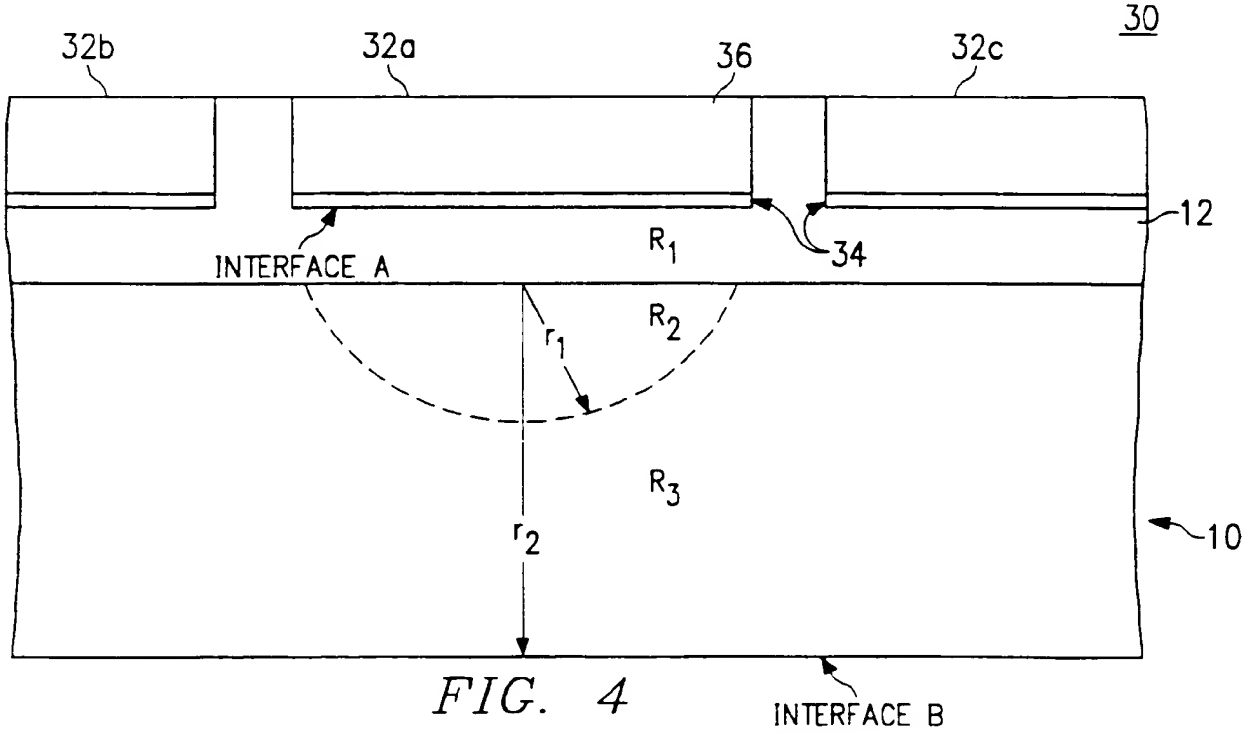

FIG. 4

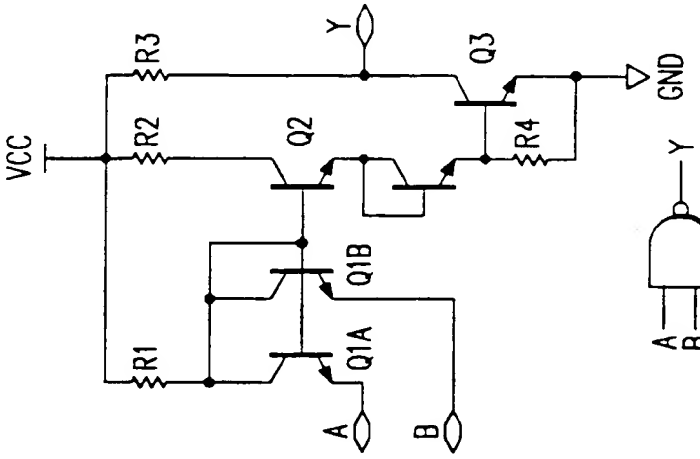

FIG. 6

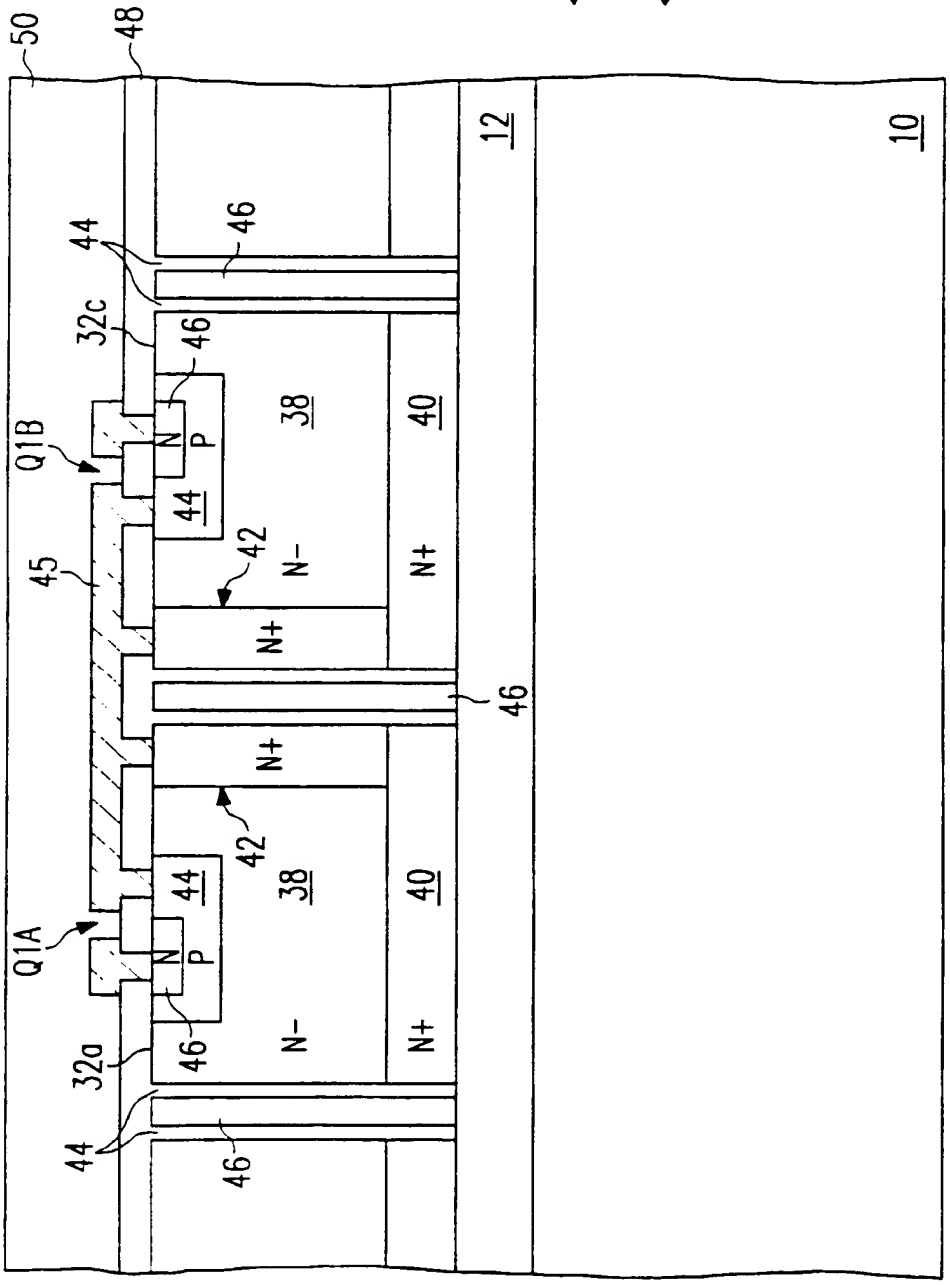

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 92/11068

A. CLASSIFICATION OF SUBJECT MATTER

IPC5: H01L 21/70, H01L 21/20, H01L 29/16
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP, A2, 0317124 (CRYSTALLUME), 24 May 1989 (24.05.89), column 4, line 48 - column 5, line 40, figures 2-3	1-8
X	WO, A1, 9111822 (ASEA BROWN BOVERI AB), 8 August 1991 (08.08.91), see the whole document	1-8
X	Appl. Phys. Lett, Volume 56, No 23, June 1990, M. I. Landstrass et al, "Total dose radiation hardness of diamond-based silicon-on-insulator structures" page 2316 - page 2318	1-8

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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INTERNATIONAL SEARCH REPORT

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4962062 (M. UCHIYAMA ET AL), 9 October 1990 (09.10.90), see the whole document	1-8
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A	US, A, 4554059 (J.P. SHORT ET AL), 19 November 1985 (19.11.85), see the whole document	1-8
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A	Proceedings of the IEEE, Volume 79, No 5, May 1991, W. Zhu et al, "Growth an Characterization of Diamond Films on Nondiamond Substrates for Electronic Applications" page 621 - page 646	1-8
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INTERNATIONAL SEARCH REPORT

Information on patent family members

01/10/93

International application No.
PCT/US 92/11068

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A2- 0317124	24/05/89	JP-A- 2110968	24/04/90
		US-A- 5131963	21/07/92
WO-A1- 9111822	08/08/91	EP-A- 0513100	19/11/92
		JP-T- 5503812	17/06/93
		SE-B,C- 465492	16/09/91
		SE-A- 9000245	25/07/91
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